AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [0026] with the following amended paragraph:

[0026] Please refer to Fig.3B with reference to Fig.3A, where Fig.3B is an equivalent circuit corresponding to the EEPROM unit depicted in Fig.3A. As shown in Fig.3B, when operated, a bit line voltage (V_{BL}) is applied to the ~~P+ doped source region 134~~ P^+ doped drain region 132 of the first PMOS transistor 101. The floating gate 122 is floating. An N-Well voltage (V_{NW}) is applied to the N-well 110. The second PMOS transistor 102 acts as a select transistor. A select gate voltage (V_{SG}) or word line voltage (V_{WL}) is applied to the select gate 124 of the second PMOS transistor 102. A source line voltage (V_{SL}) is applied to the P^+ doped source region 136 of the second PMOS transistor 102. A P-Well voltage (V_{PW}) is applied to the P-type substrate.

Please replace paragraph [0027] with the following amended paragraph:

[0027] The operation of the EEPROM according to this invention will now be described in detail with reference to an exemplary operation chart (see Fig.7), Fig.3A and Fig.3B. In Fig.7, the first (most left) column demonstrates different operation statuses including programming, reading, and erasing of the EEPROM according to this invention. The operation voltage conditions regarding writing data "1" into a selected memory cell are demonstrated in the first row of Fig.7. The operation voltage conditions regarding writing data "0" into a selected memory cell are demonstrated in the second row of Fig.7. The operation voltage conditions regarding reading data stored in memory cells are demonstrated in the third row of Fig.7. The operation voltage conditions regarding erasing data stored in memory cells are demonstrated in the fourth row of Fig.7. First, referring to the first row of Fig.7, when programming the EEPROM (writing data "1"), a relatively low-level word line voltage V_{WL} (or V_{SG}), for example, 0V, is applied to the select gate 124 of a selected EEPROM unit. A same low-level bit line voltage V_{BL} as the low-level word line voltage V_{WL}, for example, 0V, is applied to the ~~P+ doped source region 134~~ P^+ doped drain region 132 of the first PMOS transistor 101 of the selected EEPROM unit. Voltages applied to the P-type substrate 200, the N-well 110, the source line 142, and the erase gate 122 (V_{PW}, V_{NM}, V_{SL}, and V_{EG}) are 0V, 5~7V, 5~7V, and 0V, respectively. The un-selected word line is applied with a voltage ($V_{WL(un\text{-}selected)}$) having a voltage level same as V_{SL}, for example, 5~7V. The un-selected bit line is applied with a voltage ($V_{BL(un\text{-}selected)}$) having a voltage level also same as V_{SL}, for example, 5~7V. The floating gate 122 is in a floating state. As seen in the second row of Fig.7, when writing data "0" into a selected EEPROM unit, a relatively high-level bit line voltage $V_{BL(selected)}$, for example, 5~7V, is applied to the ~~P+ doped source region 134~~ P^+ doped drain region 132 of the first PMOS transistor 101 of the selected EEPROM unit.

Please replace paragraph [0031] with the following amended paragraph:

[0031] Referring to the fourth row of Fig.7 with reference to Fig.3B, when erasing the EEPROM, a relatively low-level word line voltage V_{WL} (or V_{SG}), for example, 0V, is applied. A relatively low-level bit line voltage V_{BL} of, for example, 0~-5V, is applied to the ~~P+ doped source region 134~~ P^+ doped drain region 132 of the first PMOS transistor 101. Voltages applied to the P-type substrate 200, the N-well 110, the source line 142 (V_{PW}, V_{NM}, V_{SL}) are a relatively low-level voltage of about 0V. A relatively high-level voltage, for example, an erase gate voltage V_{EG} =5~7V, is applied to the erase gate 120. The floating gate 122 is in a floating state. Erasing of the EEPROM unit 100 capitalizes on a so-called edge Fowler-Nordheim mechanism that occurs between the edge of the floating gate 122 and the subjacent erase gate 120. It is advantageous that at the very beginning stage of the erasing operation, electrons trapped in the floating gate 122 help to span bit line voltage (V_{BL}) through entire channel region under the floating gate, thereby facilitating the "pull-out" motion of the trapped electrons. On the other hand, as the erasing operation continues, the ejection or erasing rate of the trapped electrons slows down due to disappearing channel caused by reduced electrons in the floating gate 122. This is beneficial since no more mass of electrons at this stage is dragged out of the floating gate 122, that is, over-erase phenomenon of the EEPROM cells is avoided.

Please replace the Abstract with the following amended paragraph:

A single-poly EEPROM is disclosed. The single-poly EEPROM includes a first PMOS transistor that is serially connected to a second PMOS transistor. The first and second PMOS transistors are both formed on an N-well of a P-type substrate. The first PMOS transistor includes a floating gate, a first P^+ doped drain region, and a first P^+ doped source region. The second PMOS transistor includes a gate and second P^+ doped source region. The first P^+ doped ~~drain~~ source region of the first PMOS transistor serves as a drain of the second PMOS transistor. An erase gate extending to the floating gate for erasing the single-poly EEPROM is provided in the P-type substrate.

AMENDMENTS TO THE CLAIMS

Claim 1 (currently amended) A single-poly EEPROM, comprising:

a first PMOS transistor serially connected to a second PMOS transistor, wherein the first and second PMOS transistors are both formed on an N-well of a P-type substrate, and wherein the first PMOS transistor includes a floating gate, a first P^+ doped drain region, and a first P^+ doped source region, the second PMOS transistor includes a gate and second P^+ doped source region, and the first P^+ doped source region of the first PMOS transistor serves as a drain of the second PMOS transistor; and

an N-type doped region formed in the P-type substrate beneath the floating gate serving as an erase gate ~~formed in the P-type substrate~~ in the vicinity of the first PMOS transistor, wherein the floating gate of the first PMOS transistor overlaps with the N-well and the P-type substrate and extends to the erase gate.

Claim 2 (canceled)

Claim 3 (currently amended) The single-poly EEPROM of claim [[2]]1 wherein the N-type doped region formed in the P-type substrate substantially does not overlap with the floating gate.

Claim 4 (currently amended) The single-poly EEPROM of claim [[2]]1 further comprising a floating gate oxide layer between the erase gate and the floating gate.

Claim 5 (currently amended) The single-poly EEPROM of claim 1 wherein when applying a pre-selected drain bias (V_d) to the second PMOS transistor, the floating gate of the first PMOS transistor obtains an induced voltage due to capacitance coupling effects, thereby turning on a P-channel under the ~~second~~ first PMOS transistor and obtaining a gate current near a maximum value.

Claim 6 (original) The single-poly EEPROM of claim 5 wherein V_d is about –5V.

Claim 7 (original) The single-poly EEPROM of claim 1 wherein the first PMOS transistor is a single-gate transistor without any control gate formed above the floating gate of the first PMOS transistor.

Claim 8 (currently amended) The single-poly EEPROM of claim 1 wherein when ~~operating~~ erasing the single-poly EEPROM, a pre-selected erase gate bias and a ~~first doped drain region voltage~~ bit line voltage (V_{BL}) are applied to the erase gate and the first P^+ doped drain region, respectively, so as to pull trapped electrons out of the floating gate by way of FN tunneling.

Claim 9 (currently amended) The operation of single-poly EEPROM as set forth in claim

8 wherein ~~phenomenon of over-erasing is avoided~~ at a beginning stage of an erasing operation, electrons trapped in the floating gate help to span the bit line voltage (V_{BL}) through entire channel region under the floating gate, thereby facilitating "pull-out" motion of the trapped electrons, as the erasing operation continues, ejection or erasing rate of the trapped electrons slows down due to disappearing channel caused by reduced electrons in the floating gate, thereby avoiding over-erase phenomenon of the single-poly EEPROM.

Claim 10(currently amended) The single-poly EEPROM of claim 8 wherein pre-selected erase gate bias is positive, and the ~~first doped drain region voltage~~ bit line voltage (V_{BL}) is negative.

REMARKS

Claims 1 and 5-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Chang et al. USP 5,841,165. Claims 2-4 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

1. Objection to the specification:

The disclosure is objected to because of the following informalities:

A "bit line voltage (V_{BL}) is applied to the P^+ doped source region 134 of the first PMOS transistor 101" in a paragraph [0026] of a specification is contrary to "the P^+ doped drain region 132 of the first PMOS transistor 101 is electrically connected with a bit line 170 through contact plug 150" in a paragraph [0024] (see Fig.3A).

To overcome this objection, clerical errors in paragraphs [0026], [0027], and [0031] of the specification have been corrected to consist with Fig.3A. In the above-mentioned paragraphs of the specification of the present application, "P^+ doped source region 134" is replaced with "P^+ doped drain region 132", as seen in the above AMENDMENT section. No new matter has been introduced by this amendment, consideration of which is politely requested.

2. Rejection of claim 1 under 35 U.S.C. 102(b):

Claim 1 is rejected under 35 U.S.C. 102(b), for reasons of record that can be found on pages 2-3 in the Office action identified above, which is part of paper no.2.

To overcome this rejection, claim 1 has been amended. The limitation in claim 2 that is found allowable by the Examiner is now merged into claim 1. No new matter is entered. Reconsideration of the amended claim 1 is therefore politely requested.

None of the prior arts discloses "*an N-type doped region formed in the P-type substrate beneath the floating gate serving as an erase gate in the vicinity of the first PMOS transistor*", as required by the amended claim 1. Accordingly, the Applicants suggest that the amended claim 1 is now in condition for allowance, and such action is therefore respectfully requested.

3. Amendment to claim 9:

Claim 9 is amended based on the context as set forth in the paragraph [0031] on pages 8 and 9 of the specification of the present application for emphasizing the features of this invention. No new matter is introduced.

It is respectfully suggested that none of the cited references, alone or in combination, teach or make obvious all of the limitations of the amended claim 9. Reconsideration of the amended claim 9 is therefore politely requested.

4. Rejection on claims 5-9 and objection over claims 2-4 and 10:

Claims 5-9 are rejected under 35 U.S.C. 102(b). Claims 2-4 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening

claims.

Accordingly, claim 2 has been merged into claim 1 and has therefore been canceled in this amendment. As claims 3-10 are dependent upon the amended independent claim 1, they should be allowable if the amended claim 1 is allowed. Reconsideration of claims 3-10 is therefore politely requested.

Sincerely yours,

Winston Hsu

Date: 9/17/2003

Winston Hsu, Patent Agent No.41,526
P.O. BOX 506
Merrifield, VA 22116
U.S.A.
e-mail: winstonhsu@naipo.com.tw